

CLAIMS

What is claimed is:

- 1 1. A computer system which includes an apparatus for monitoring the
2 performance of a multithreaded processor, said apparatus comprising:
3 a processor adapted to execute a plurality of threads simultaneously,
4 each thread including a series of instructions;
5 a plurality of programmable event counters to count two or more
6 independent events generated by one or more threads of said plurality, said
7 two or more events selected from a predetermined list of events resulting
8 from the normal operation of said processor;
9 one or more registers to control the operation of said event counters,
10 each register also selecting the events to be counted from said list of events;
11 and
12 an access location to allow access to said event counters to determine
13 a current count of said events.

- 1 2. The computer system of claim 1 wherein said access location allows
2 access to determine said count without disturbing the operation of said
3 counters.

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1 3. The computer system of claim 2 wherein each register comprises a
2 first field of bits for choosing one or more events to be counted.

1 4. The computer system of claim 3 wherein each register further
2 comprises a second field of bits for choosing one or more events to be
3 masked and not counted.

1 5. The computer system of claim 4 wherein each register further
2 comprises a third field of bits for choosing from which of said plurality of
3 threads an event is to be counted according to each thread's ID.

1 6. The computer system of claim 5 wherein said third field of bits can
2 further choose from which of said plurality of threads an event is to be
3 counted according to each thread's current privilege level (CPL).

1 7. The computer system of claim 6 wherein said counters can be
2 stopped and cleared before a new event is selected.

1 8. The computer system of claim 7 wherein said counters can be preset
2 to a certain state.

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1 9. The computer system of claim 5 wherein said predetermined list of
2 events includes hardware performance and breakpoint events.

1 10. An apparatus for monitoring the performance of a multithreaded
2 processor comprising:

3 processing means for processing a plurality of threads simultaneously,
4 each thread including a series of instructions;

5 counting means for counting one or more events generated by one or
6 more threads of said plurality, said one or more events selected from a
7 predetermined list of events resulting from the normal operation of said
8 processor;

9 controlling means for controlling said counting means and for
10 choosing said one or more events from said list; and

11 accessing means for accessing said counting means to determine the
12 count of said one or more events.

1 11. The apparatus of claim 10 wherein said counting means comprises a
2 plurality of programmable counters.

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1 12. The apparatus of claim 11 wherein said controlling means comprises
2 one or more registers, each register including a first field of bits for choosing
3 one or more events to be counted.

1 13. The apparatus of claim 12 wherein each register further comprises a
2 second field of bits for choosing one or more events to be masked and not
3 counted.

1 14. The apparatus of claim 13 wherein each register further comprises a
2 third field of bits for choosing from which of said plurality of threads an event
3 is to be counted according to each thread's ID.

1 15. The apparatus of claim 14 wherein said third field of bits can further
2 choose from which of said plurality of threads an event is to be counted
3 according to each thread's current privilege level (CPL).

1 16. The apparatus of claim 15 wherein said accessing means comprise
2 instruction means within said processor for reading a count from each of said
3 counters.

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1 17. The apparatus of claim 14 wherein said predetermined list of events
2 includes hardware performance and breakpoint events.

1 18. A method for monitoring the performance of a multithreaded
2 processor, said method comprising:
3 executing a plurality of threads simultaneously, each thread including
4 a series of instructions;

5 counting a plurality of independent events generated by one or more
6 threads of said plurality, said plurality of events selected from a
7 predetermined list of events resulting from the normal operation of said
8 processor;

9 controlling the operation of said event counters, each register also
10 selecting the events to be counted from said list of events; and
11 accessing said event counters to determine a current count of said
12 events.

1 19. The method in claim 18 further comprising:
2 prior to said counting, selecting and qualifying said plurality of
3 independent events to be counted.

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1 20. The method in claim 19 wherein said qualifying includes requiring that
2 said plurality of events have a preselected thread ID.

1 21. The method in claim 20 wherein said qualifying further includes
2 requiring that said plurality of events have a preselected thread current
3 privilege level (CPL).

1 22. An apparatus incorporated in an integrated circuit (IC) for monitoring
2 the performance of a multithreaded central processing unit (CPU) by
3 recording the occurrence of events resulting from the normal operation of
4 said CPU, each event comprising an electric signal representing the
5 incidence of a particular activity within said IC, said apparatus comprising:

6 a processor adapted to execute a plurality of threads simultaneously,
7 each thread including a series of instructions

8 first and second programmable counters operated synchronously to
9 record first and second selected events respectively;

10 logic circuitry to couple said first and second selected events to said
11 first and second programmable counters, respectively;

12 a control register coupled to said logic circuitry to select said first and
13 second selected events; and

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14 an access location to allow access to said counters.

1 23. The apparatus of claim 22 wherein said logic circuitry comprises one
2 more multiplexers coupled to receive a plurality of events.

1 24. The apparatus of claim 23 wherein said logic circuitry is adapted to
2 select said first and second selected events from said plurality of events
3 according to their thread ID.

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